Building the Digital Future

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September 12, 2002

Intel Developer Forum Fall 2002


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Yesterday's Dreams

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Discovering Pathways

Alan Kay

"The best way to predict the future is to invent it."

"Nanotechnology offers... possibilities for health, wealth, and capabilities beyond most past imaginings "

Eric Drexler

Neil Gershenfeld

"... our goal is to embed intelligence into everyday objects... "

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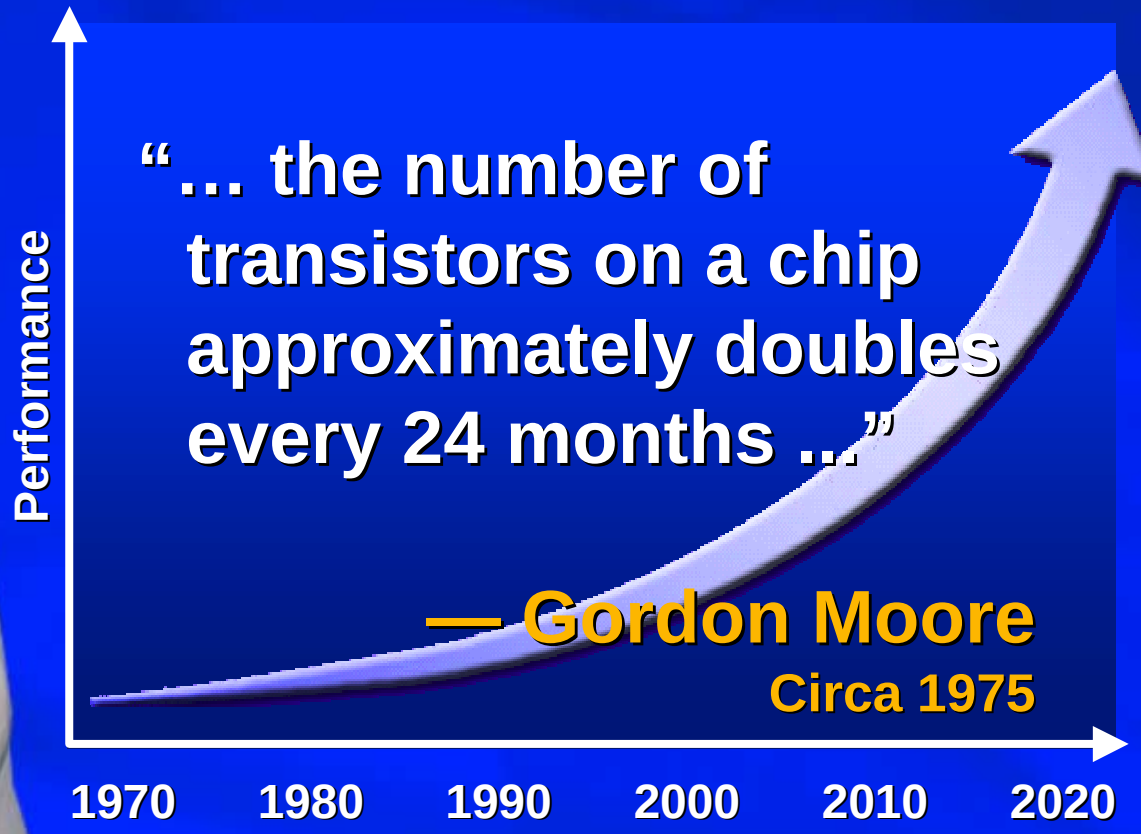

Video

Intel Developer Forum Fall 2002


The Digital Future
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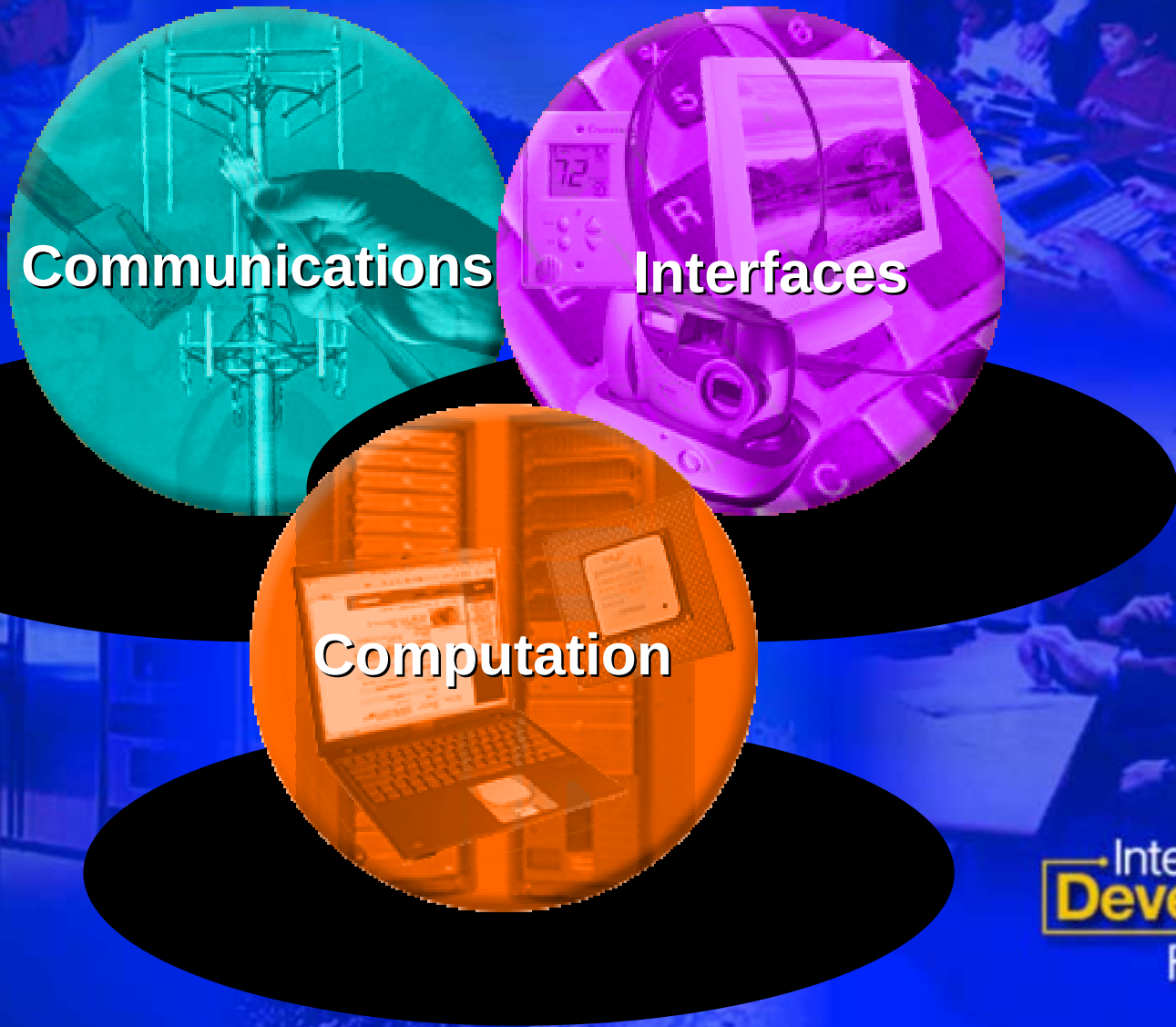
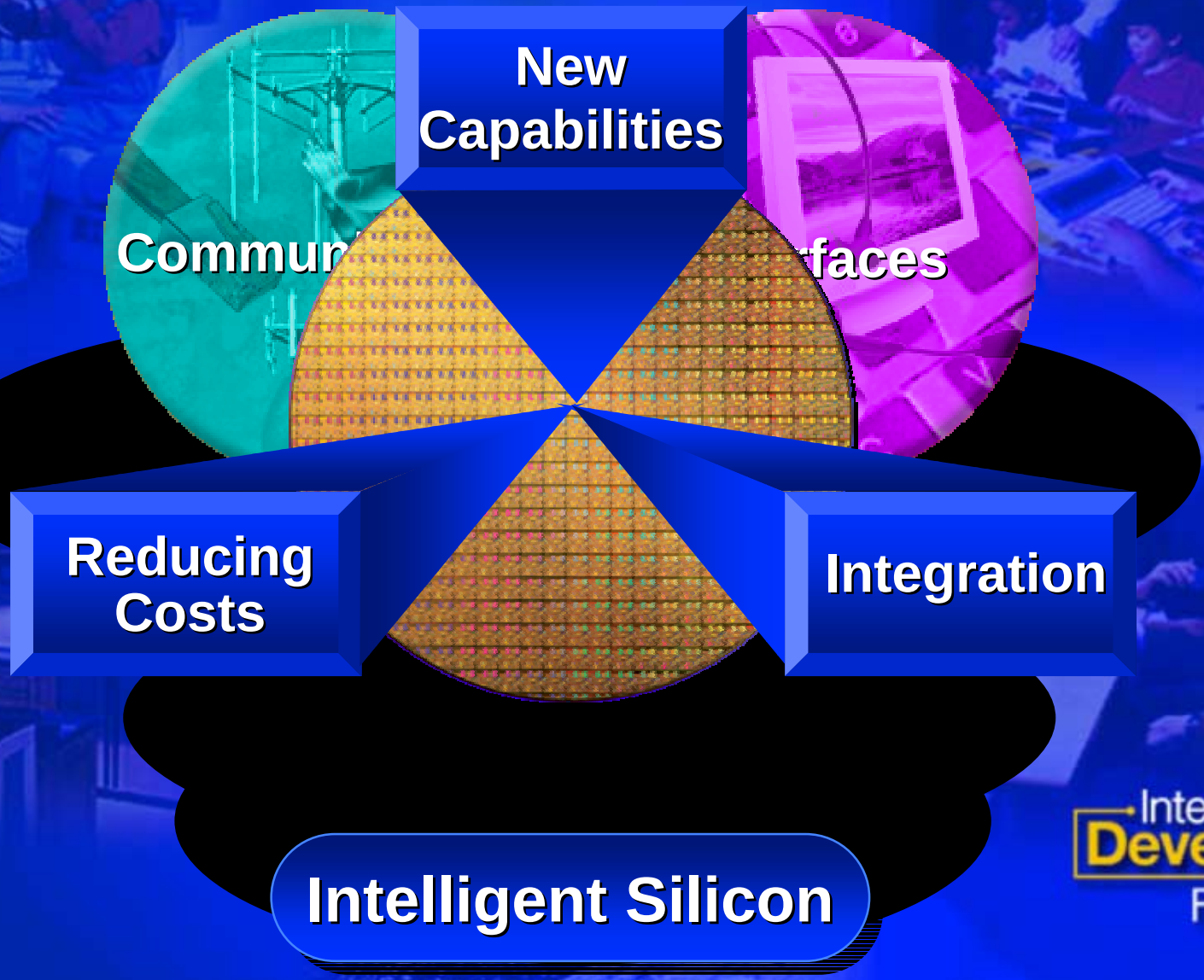
Bridge to the Digital Future



Silicon: The Underlying Trajectory



Moore's Law: Industry Guidepost

EXTENDING

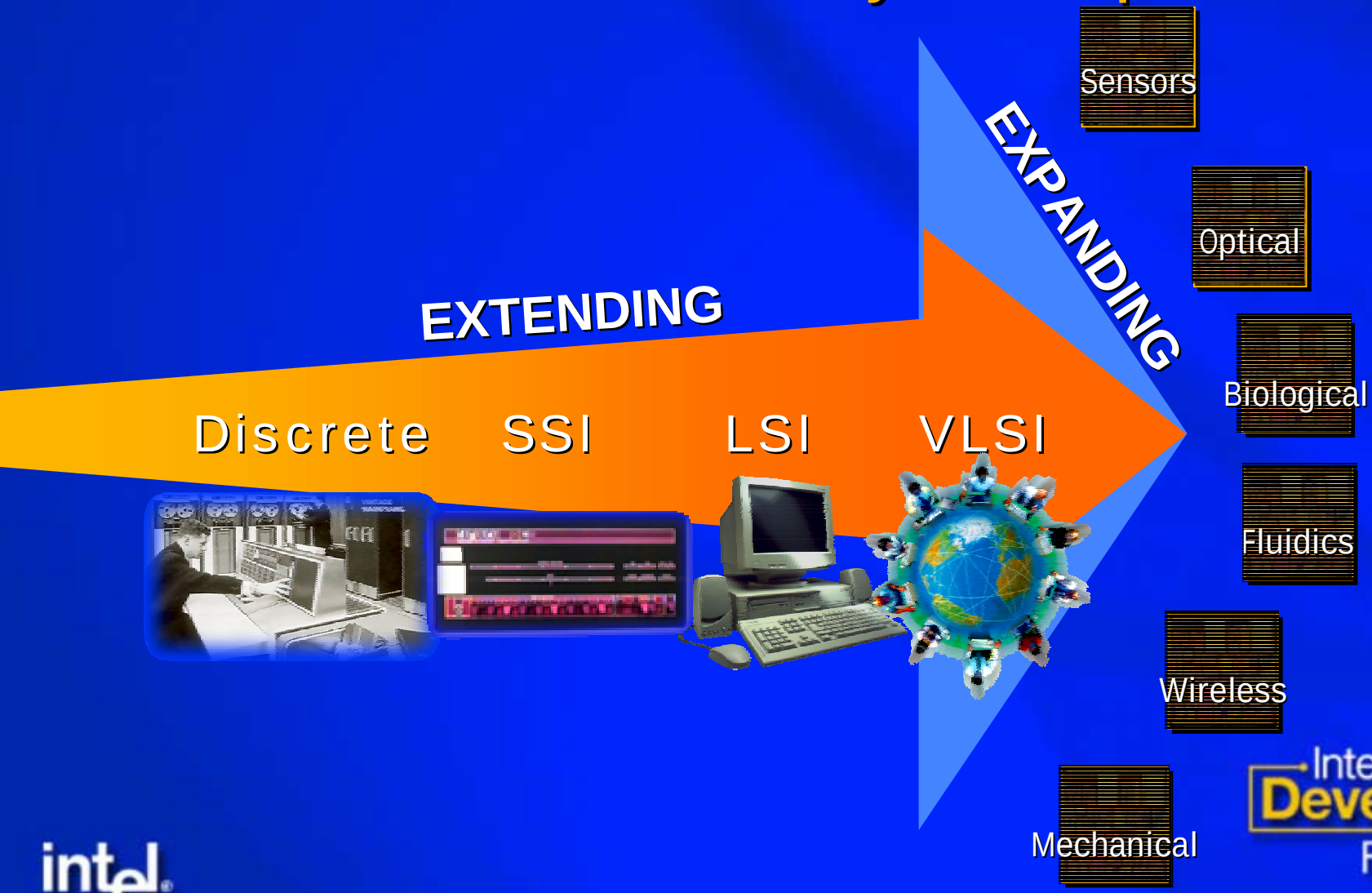
Discrete

Moore's Law: Industry Guidepost

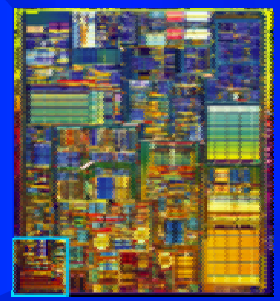
Moore's Law: Industry Guidepost

Moore's Law: Industry Guidepost

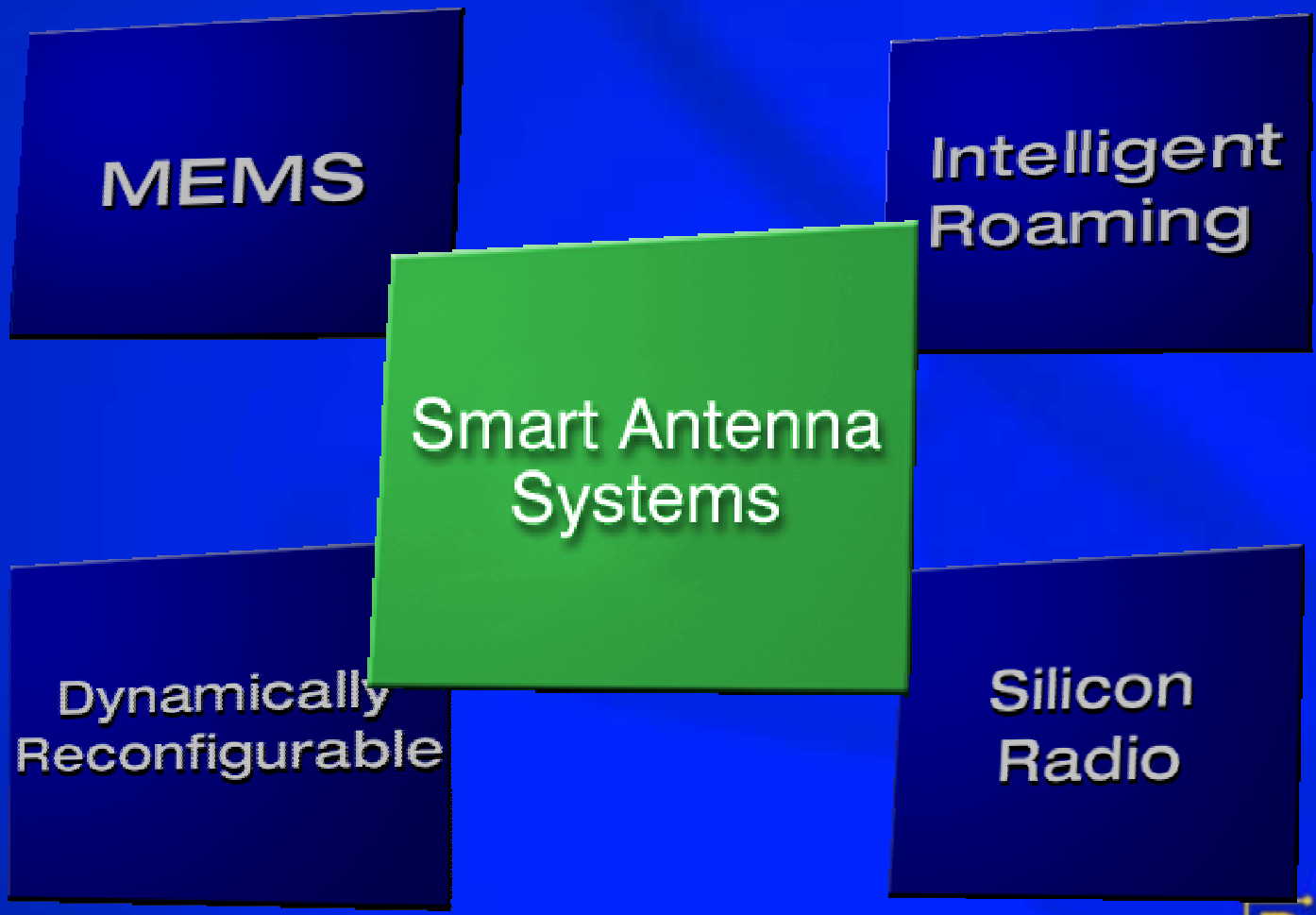
Moore's Law: Industry Guidepost



“Radio Free Intel”



“Radio Free Intel”: Research Areas



Smart Multiple-Antenna Systems

Complex Scheduling/Encoding	Signal Processing Antenna Control	Benefits
Spatial Frequency Time	Phase Amplitude	Capacity Throughput Coverage Reliability

Silicon Photonics

TODAY

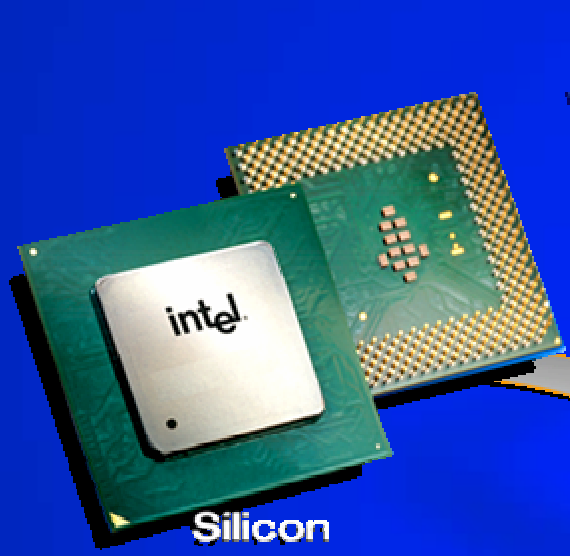
Silicon Electronics

Moore's Law
– Intel Does it Best

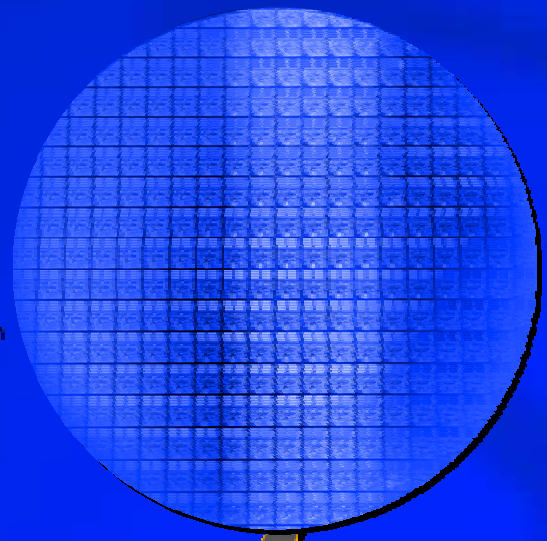
RESEARCH

Silicon Photonics

Silicon-based Optical Building Blocks



Silicon Processor



- WAVE GUIDES
- FILTER
- MODULATOR
- FAST SWITCH
- PHOTO DETECTOR

Integrated Electronics and Photonics

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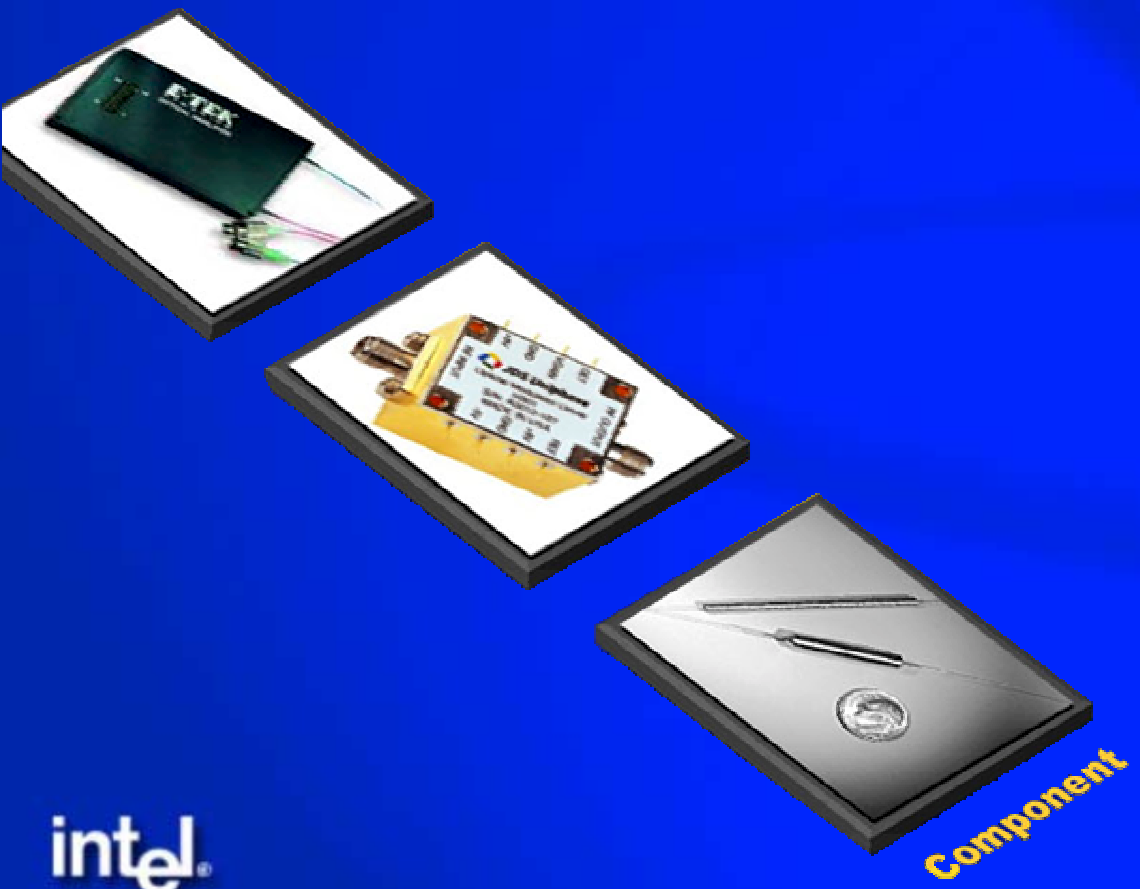
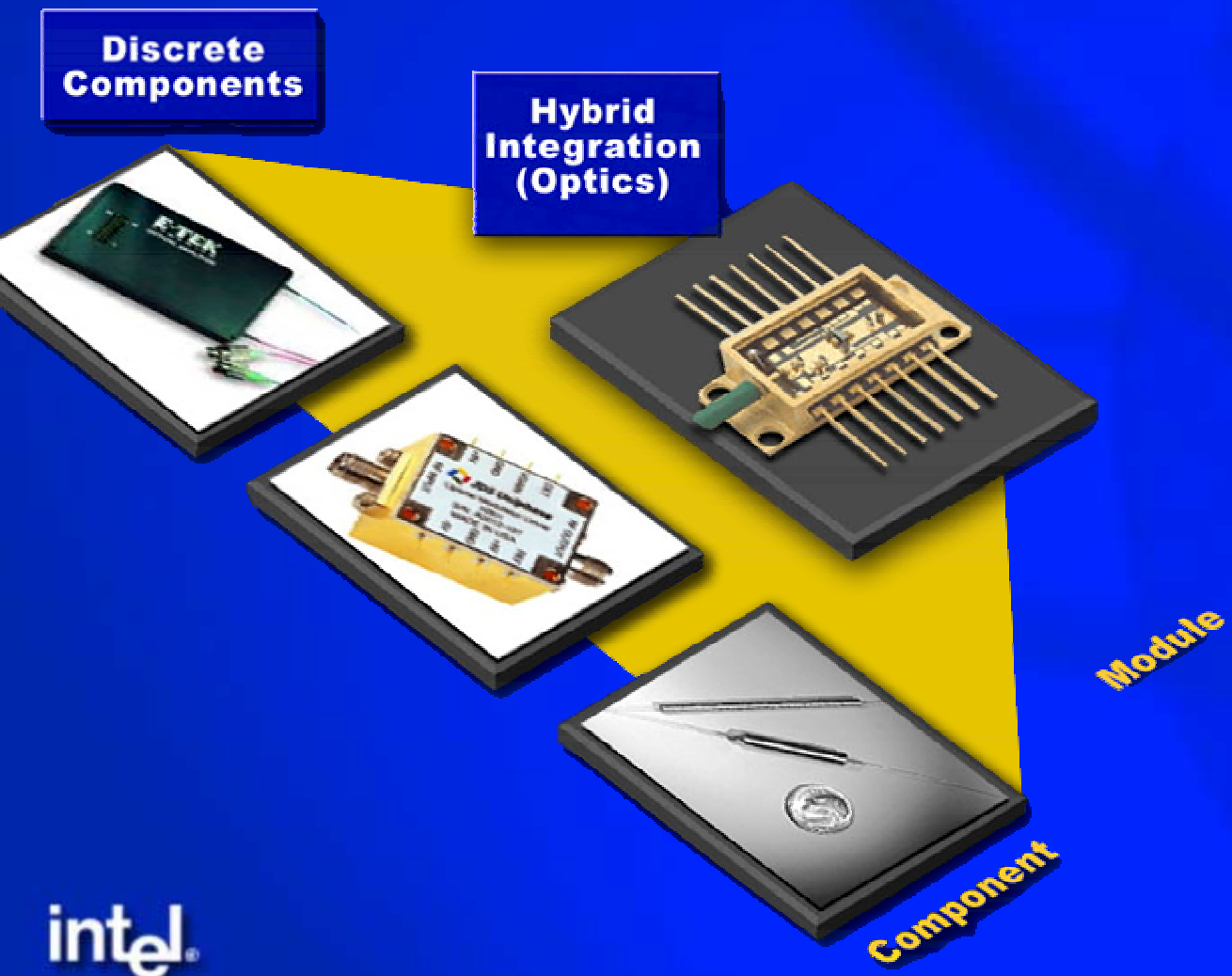
Next Steps: Integration Phases

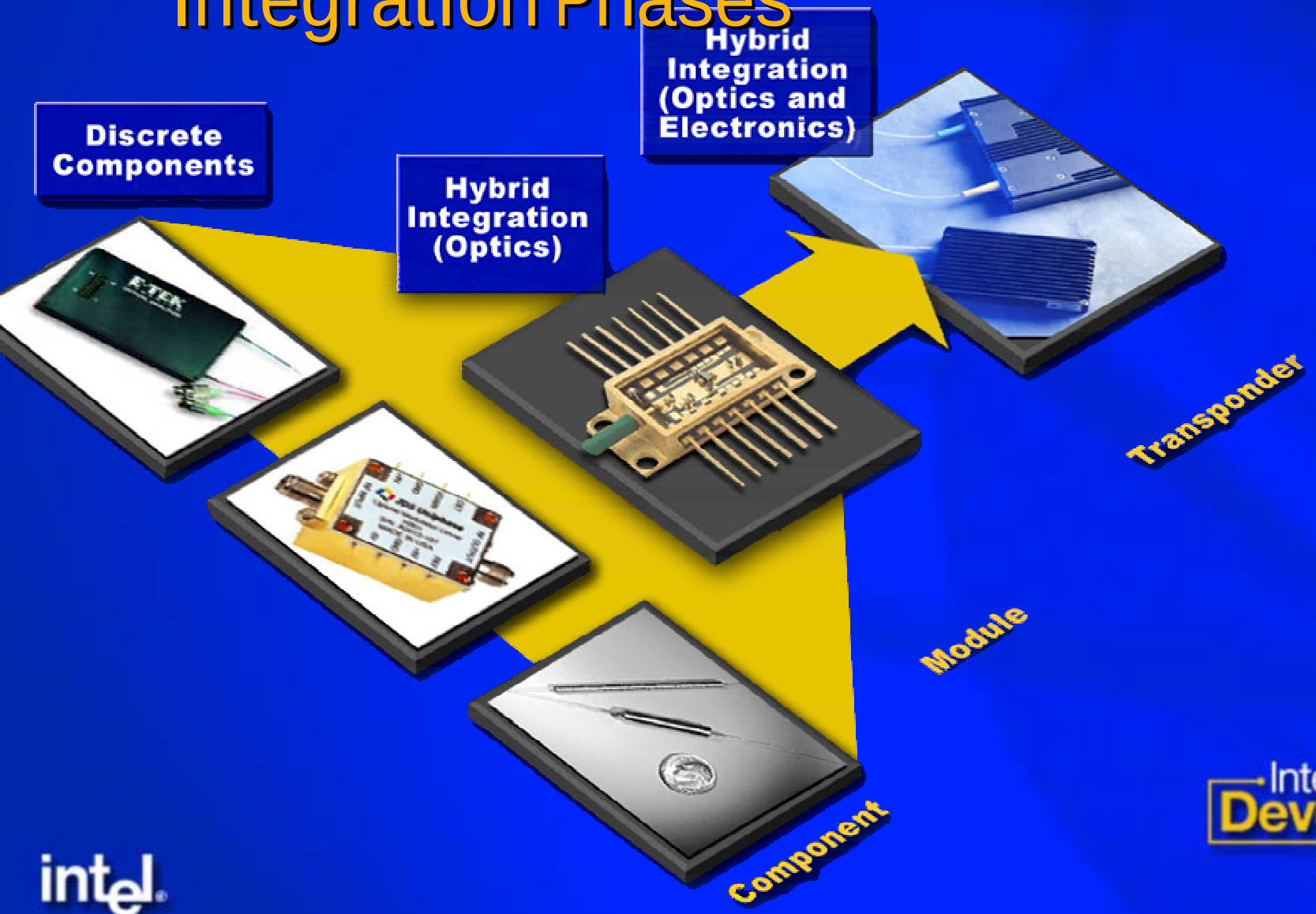
Discrete Components



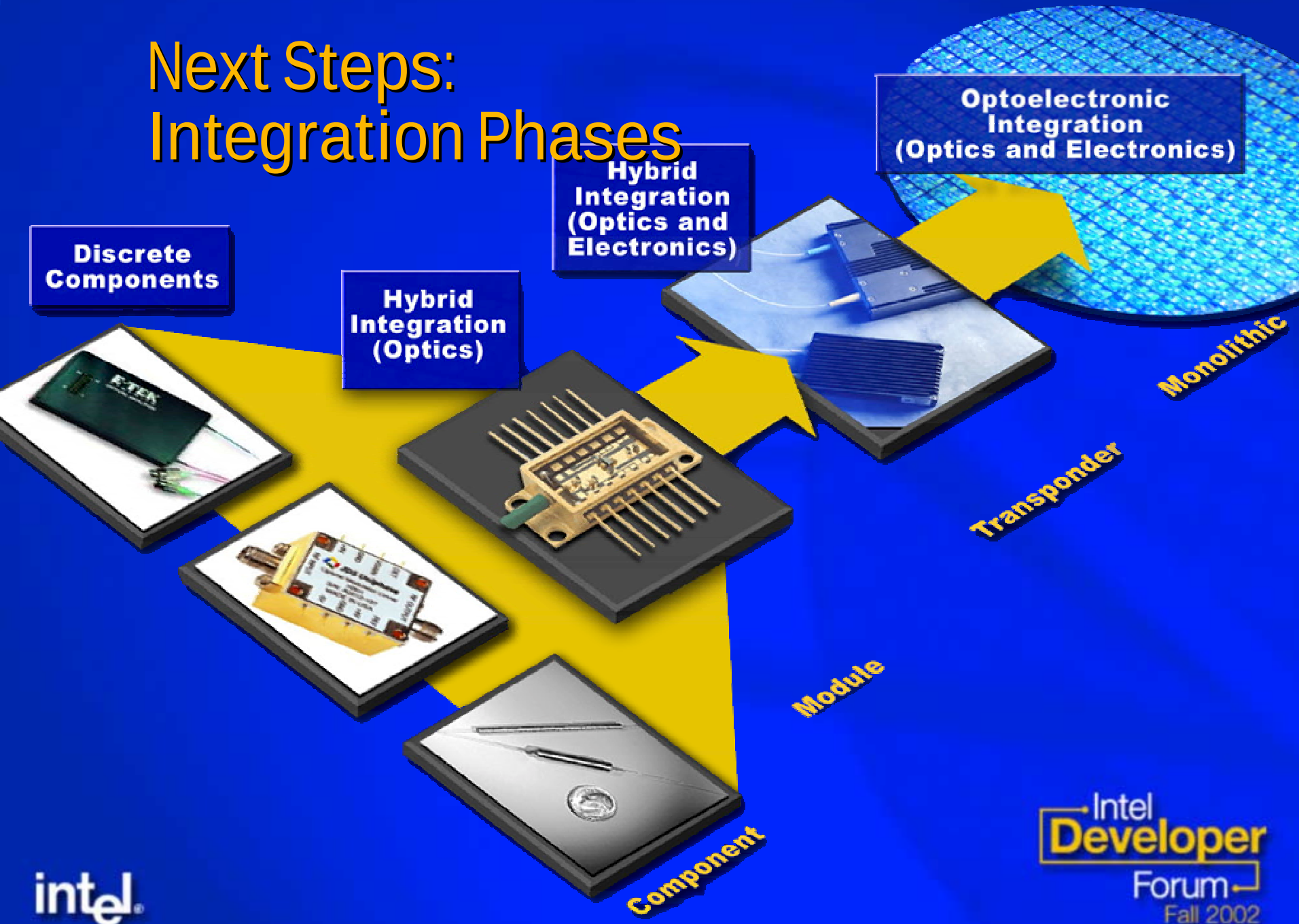
Next Steps: Integration Phases



Next Steps: Integration Phases



Next Steps: Integration Phases



Sensor Networks

Sensor Networks

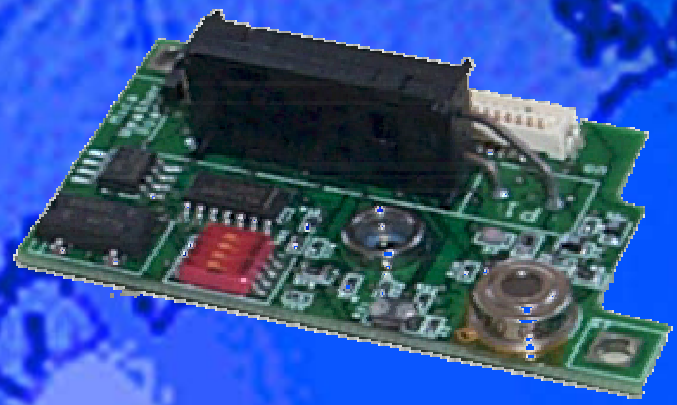
Sensing +

Computing +

Communicating

Communications-Computing

Great Duck Island Deployment



Great Duck Island

Programming Sensor Networks Research

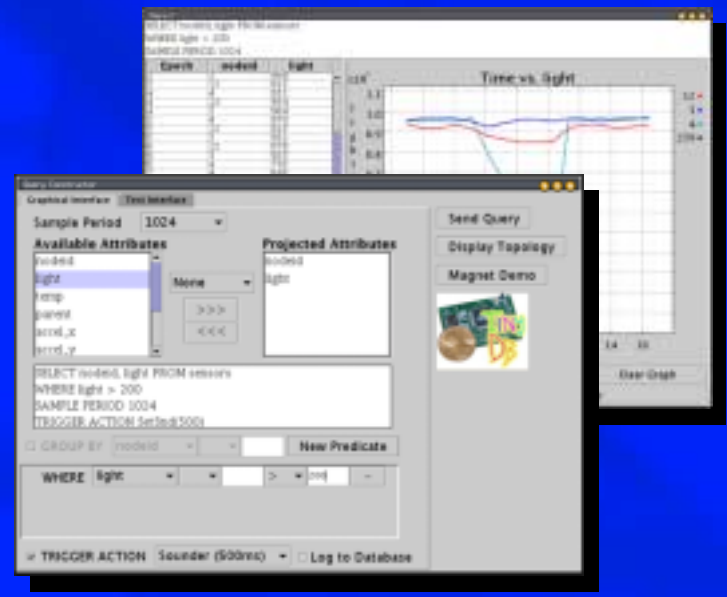
TinyOS

a component-based OS for the networked sensor regime

http://webs.cs.berkeley.edu

Berkeley

University of California



http://berkeley.intel-research.net/tinydb/

TinyDB: In-Network Query Processing in TinyOS

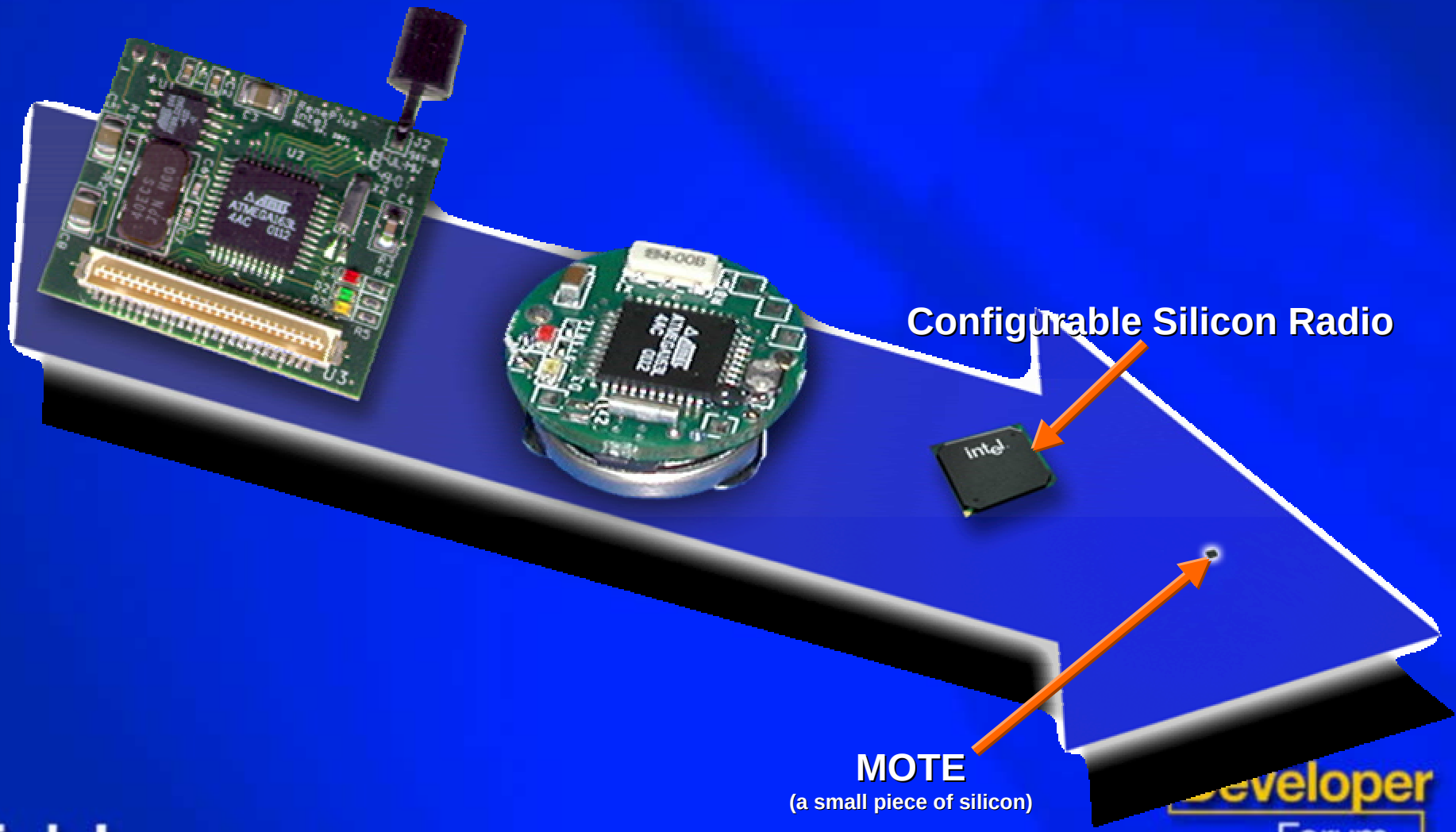
Samuel Madden, Joe Hellerstein, and Wei Hong

IRB-TR-02-014

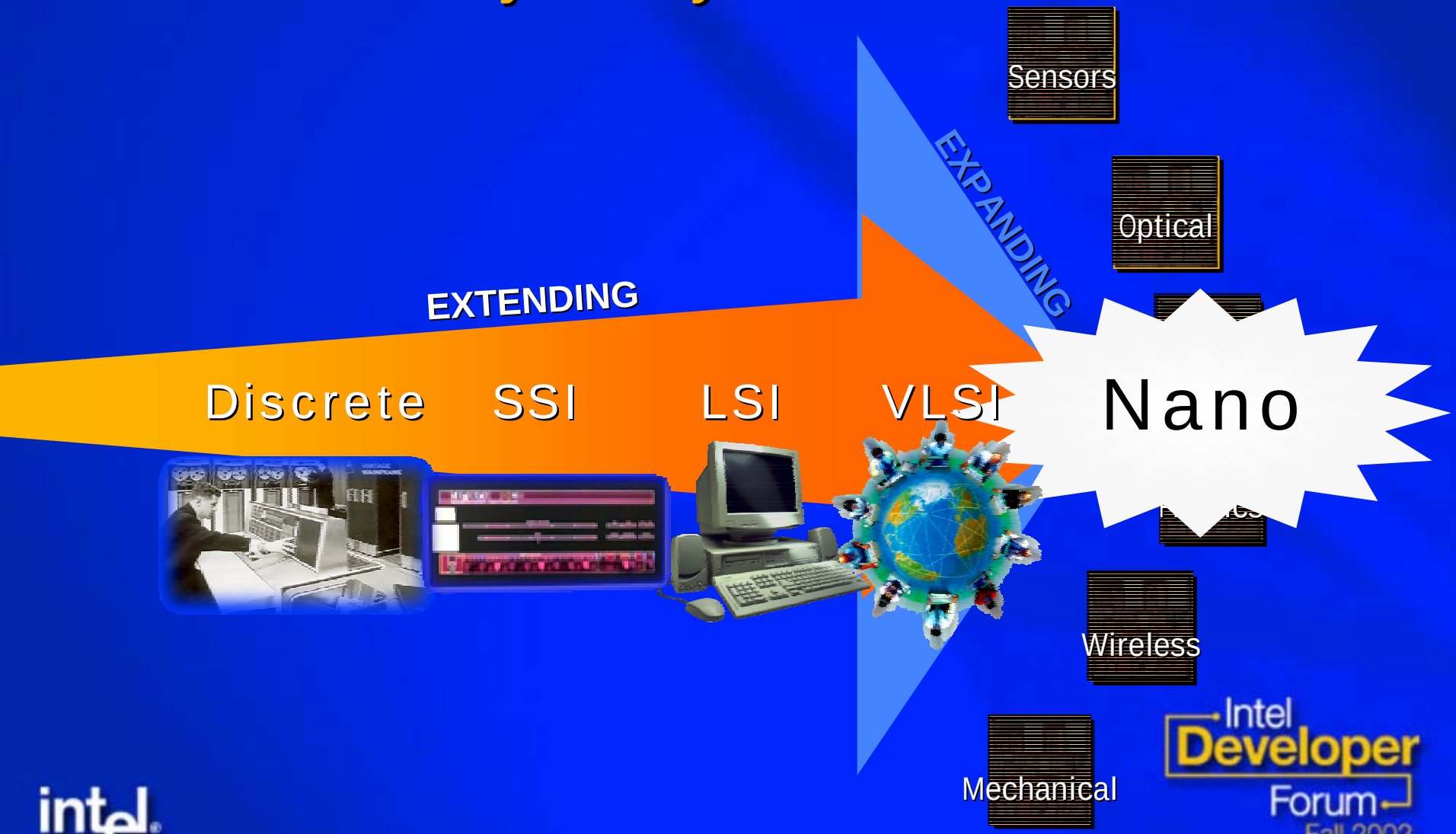
August, 2002

Intel Developer Forum Fall 2002

iMote Research



Silicon Trajectory



What is Nanotechnology?

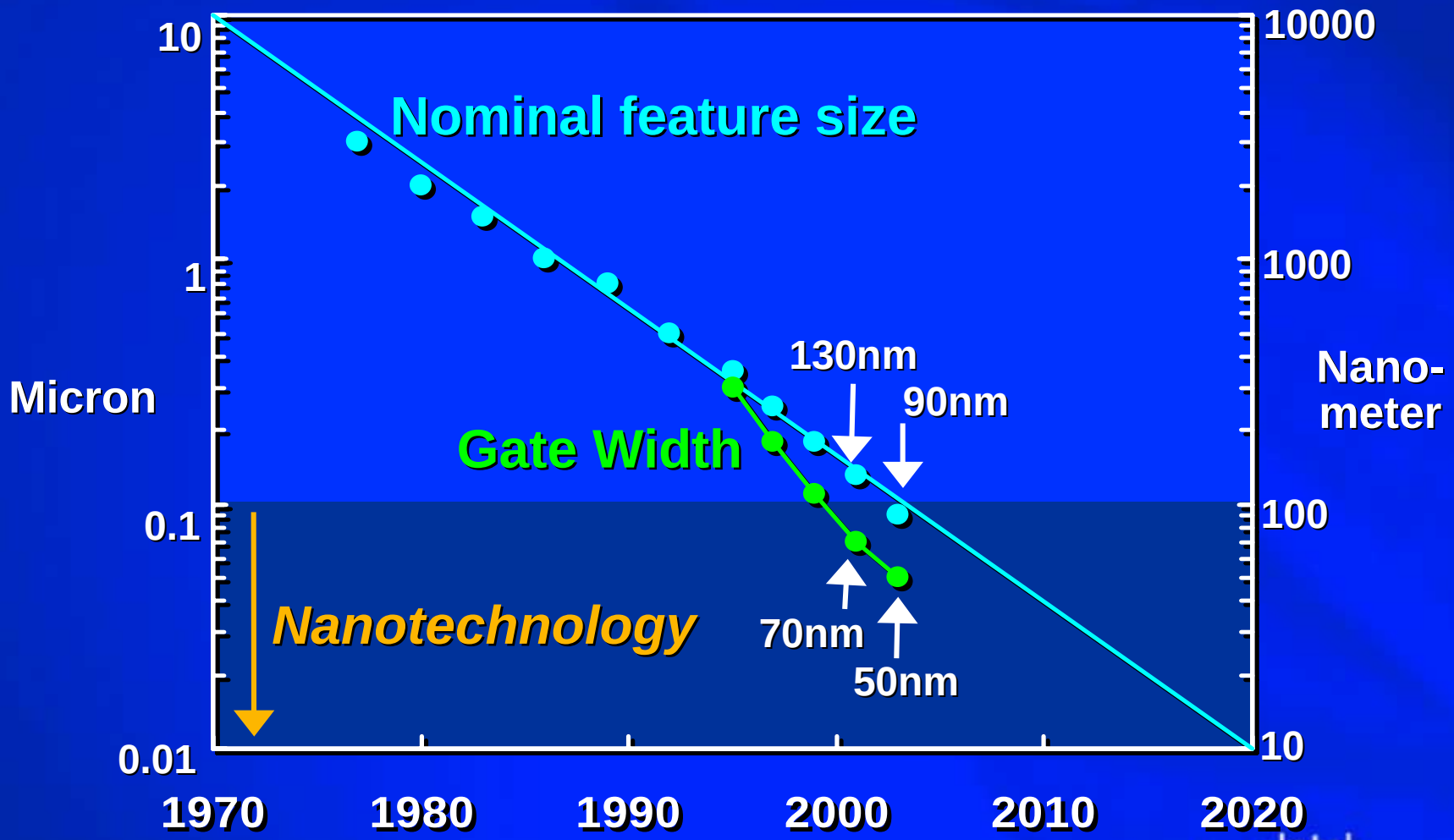
a. New structures like carbon nanotubes
b. Silicon devices made smaller
c. Arranging atoms and molecules
d. Letting atoms assemble themselves
e. Something far in the future
f. In production today
g. All of the above

Correct answer: g.

Nanotechnology features

- **Structures measured in nanometers**
  - **Less than 0.1-micron (100nm)**
- **New materials and device structures**
  - **Incrementally changing silicon technology base**
- **Materials manipulated on atomic scale**
  - **In one or more dimensions**
- **Increasing use of self-assembly**
  - **Using chemical properties to form structures**

Silicon Nanotechnology is Here!



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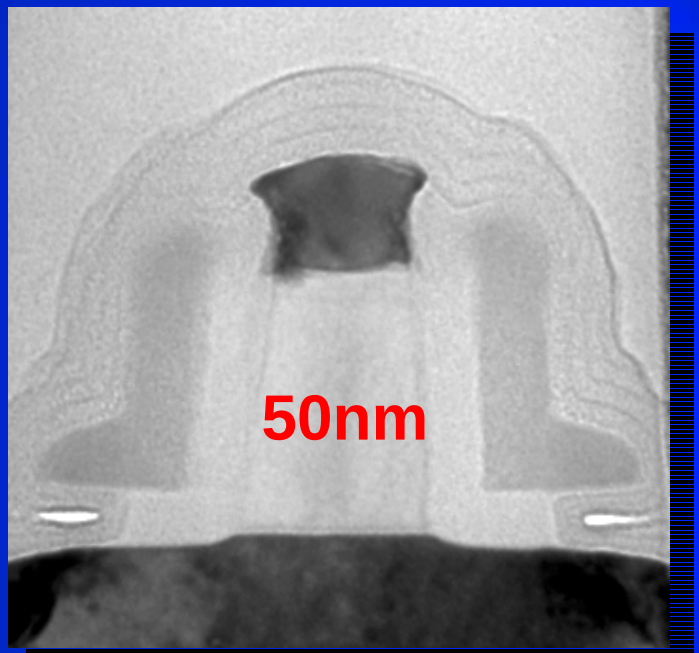
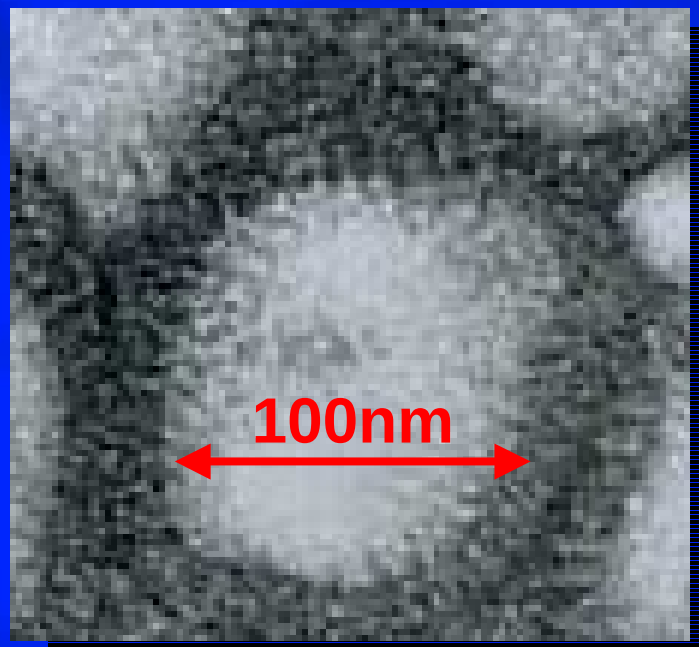
Silicon Devices Shrink to Virus Size



Transistor for 90nm Process

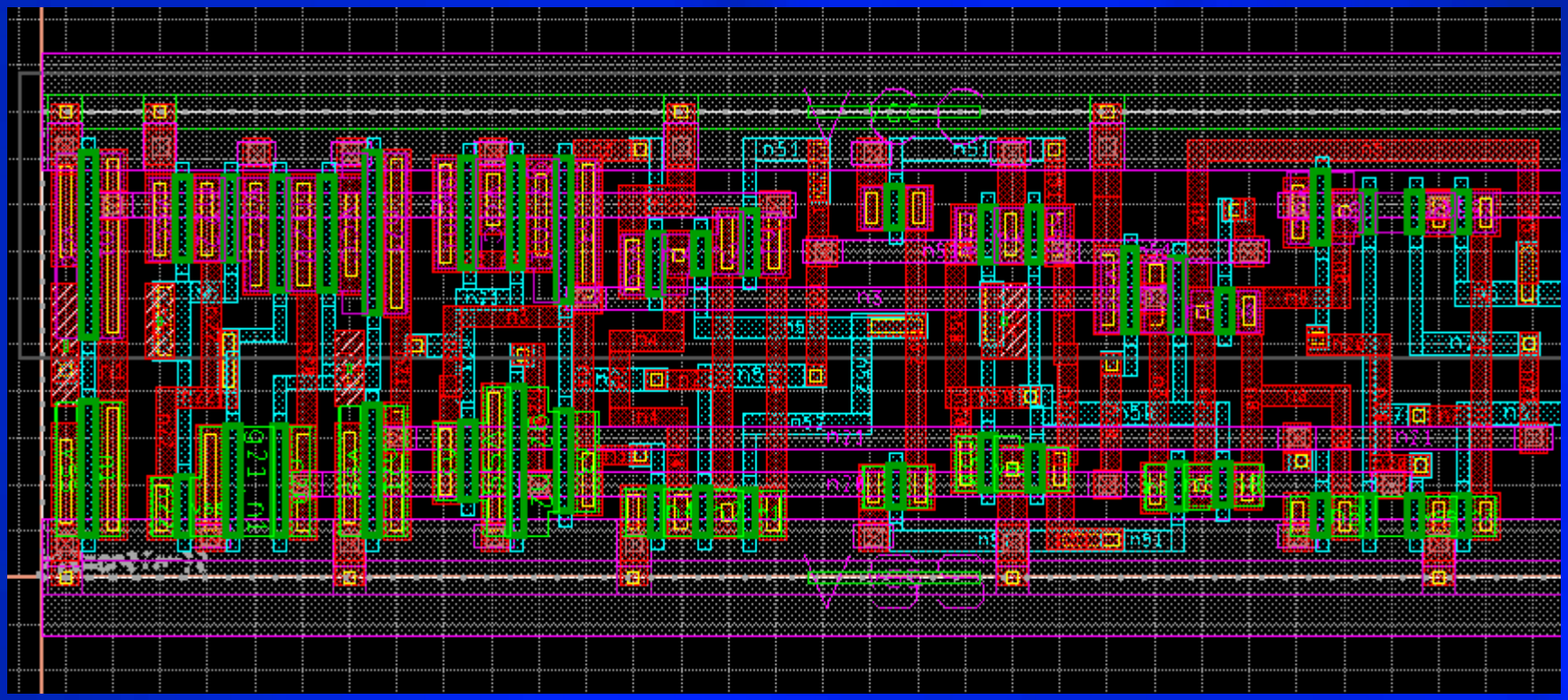
Source: Intel



Influenza virus

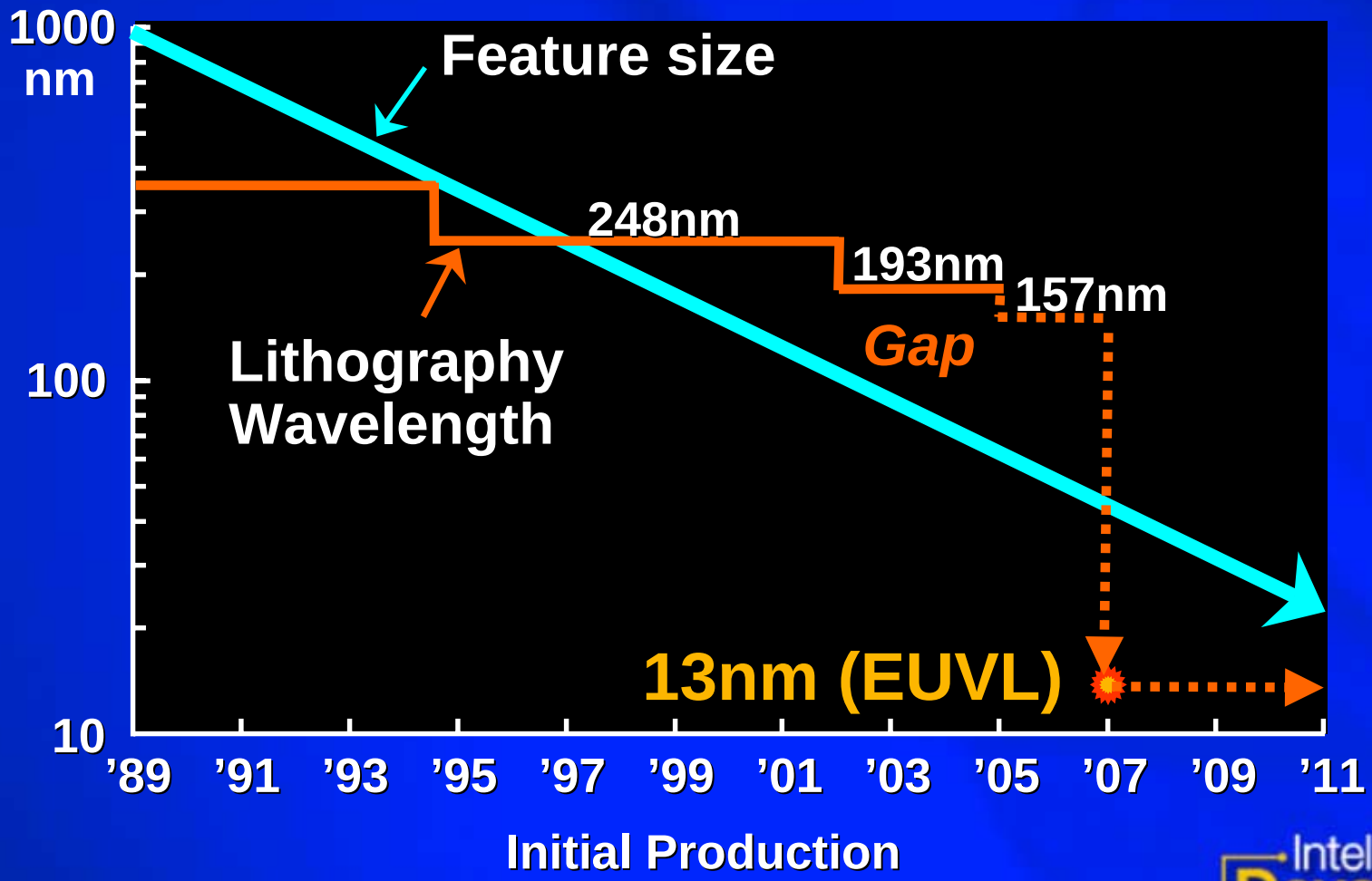
Source: CDC

Lithography is the Designer's "Brush"

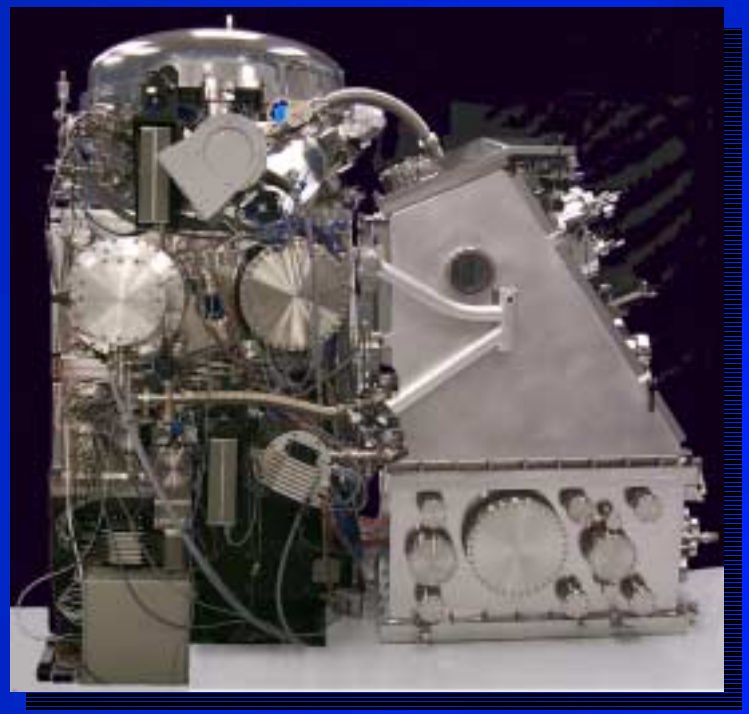


Lithography is indispensable for defining locations/configurations of circuit elements/functions

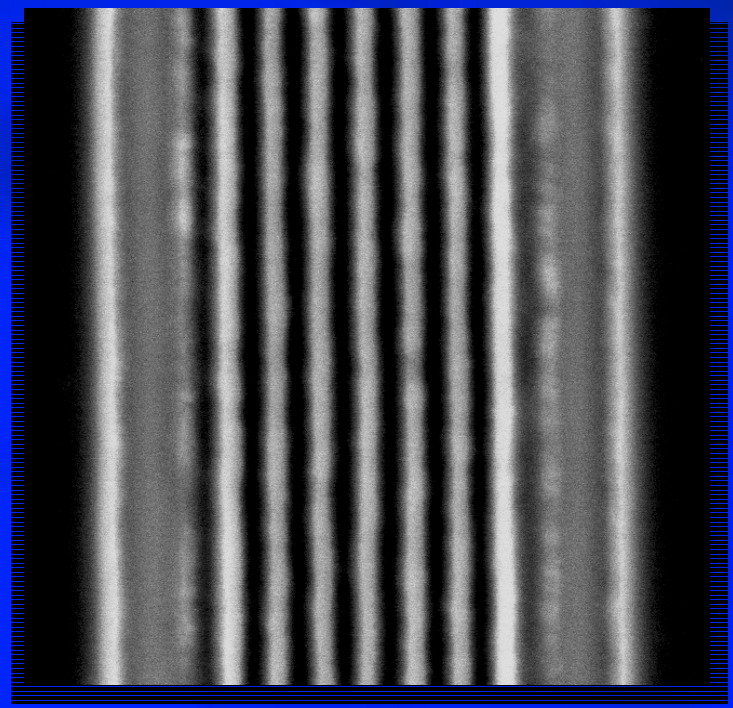
Lithography Gap to Close with EUVL



EUV LLC Consortium Demonstrates EUVL



EUV Lithography Prototype Exposure Tool



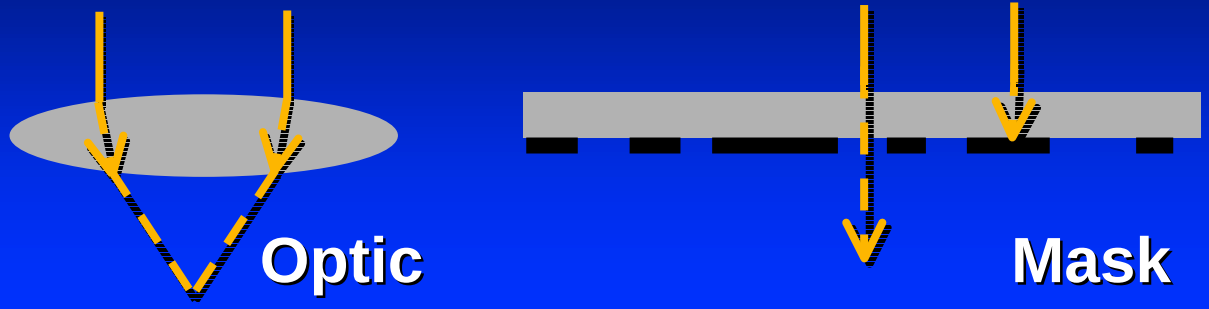
50nm Lines Printed with EUV Lithography

Source: Sandia

EUV lithography is now in commercialization phase

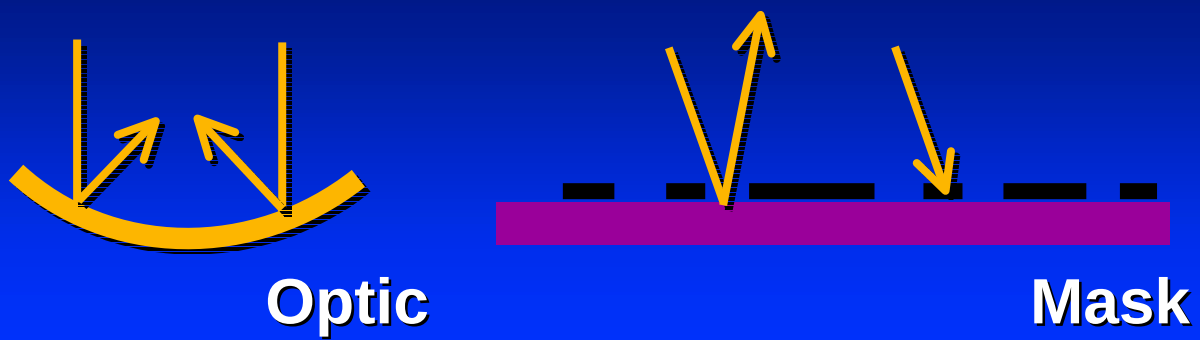
EUVL Overcomes Optical Materials Limits

Conventional lithography (refractive)



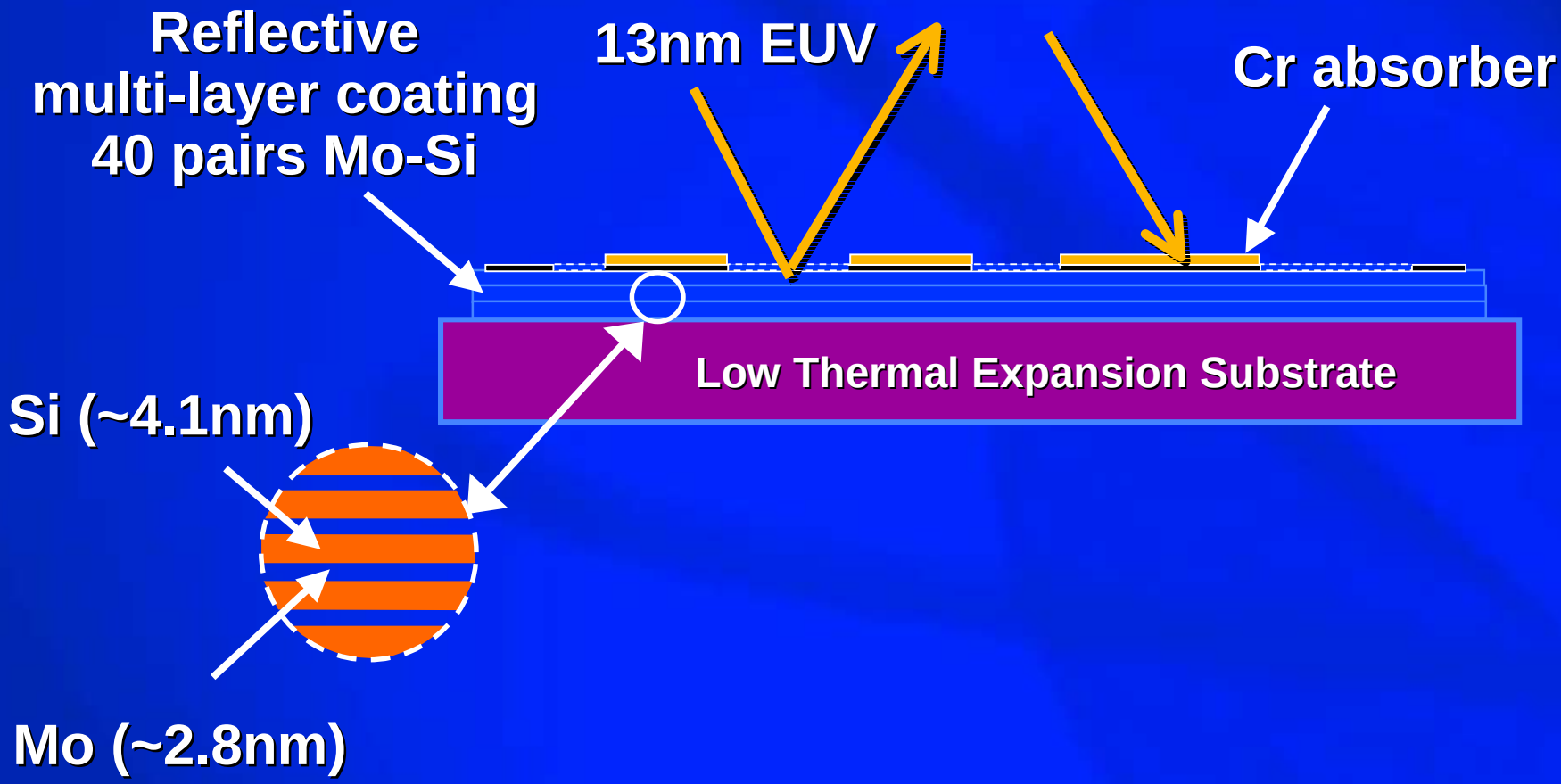
Optical materials do not transmit short wavelengths

EUV lithography (reflective)



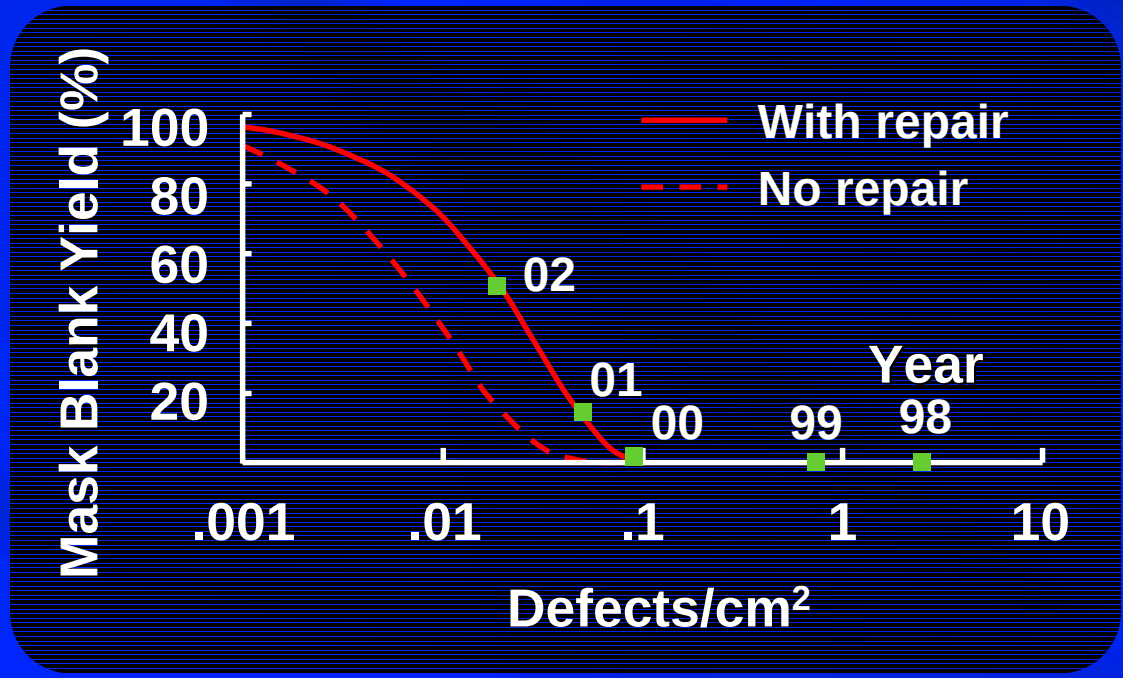
Multi-layer coating reflects short wavelengths

EUV Reflective Mask Structure



EUV Mask Yield Breakthroughs

EUV Mask



New Materials, Devices Extend Si Scaling

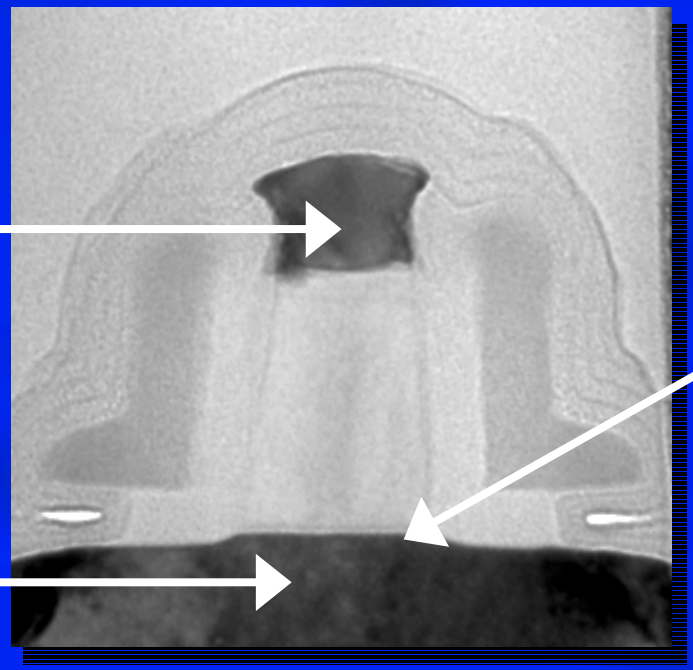
Changes Made

Gate

Silicide added

Channel

Strained silicon



Transistor

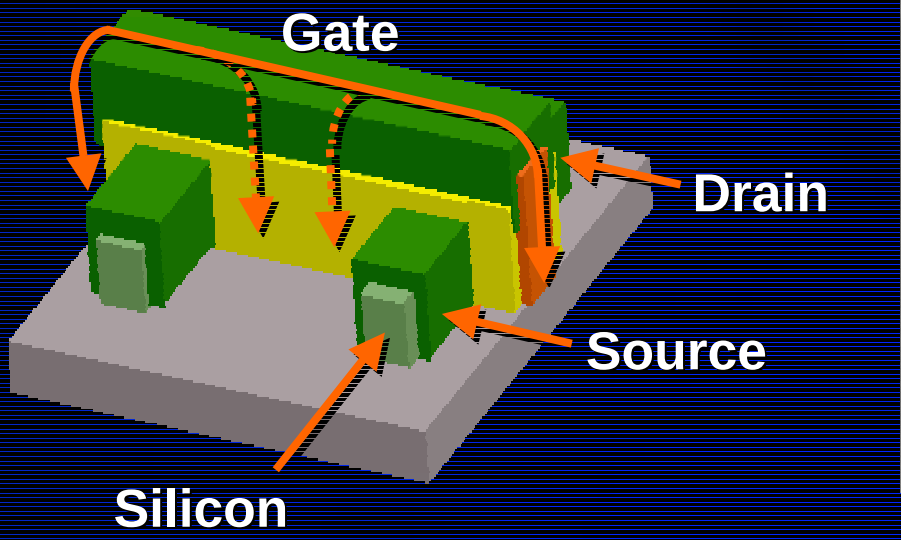
Future Options

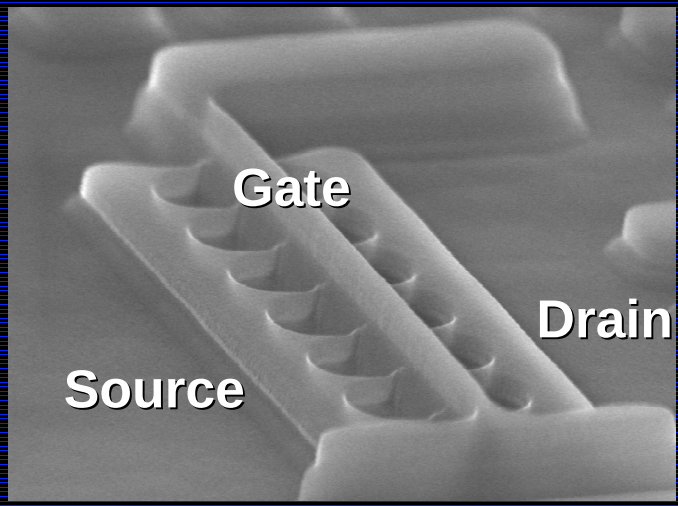
High-k gate dielectric

New transistor structure

Source: Intel

Experimental Tri-Gate Transistor





Source: Intel

- Improved version of TeraHertz transistor
  - Better performance
  - Scalable to smaller sizes
- Technical details to be presented
  - ISSDM Conference, Japan, Sept 17, 2002

New Materials, Devices Extend Si Scaling

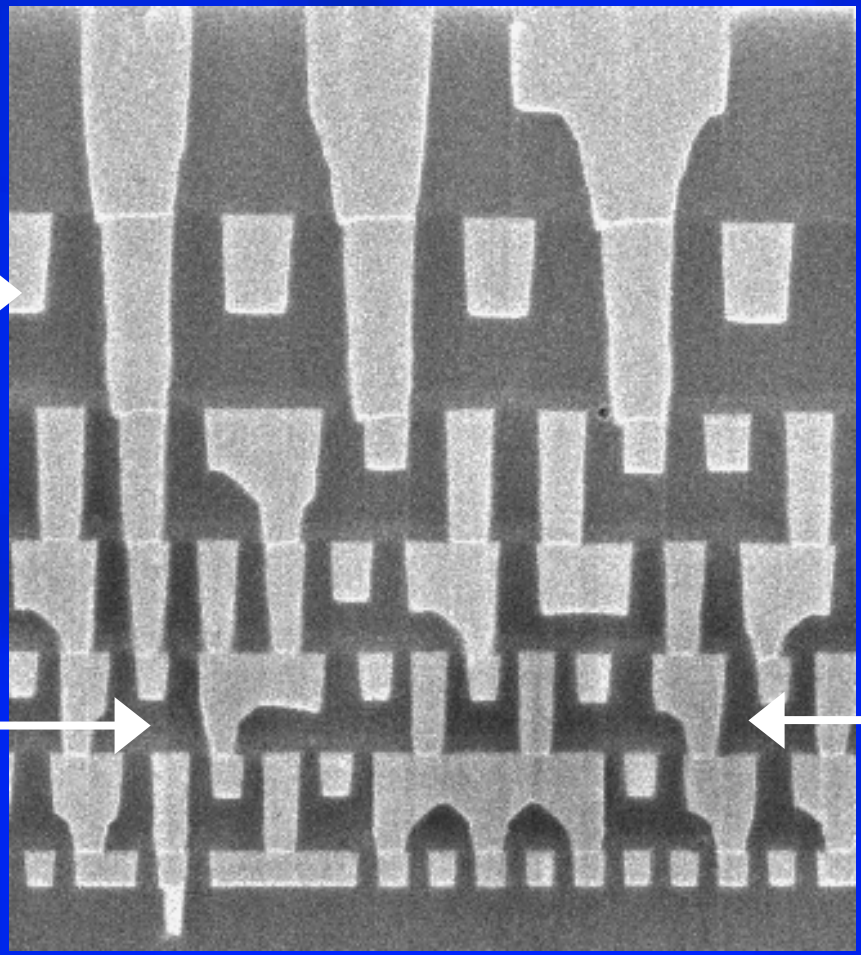
Changes Made

Metal lines

Al → Cu

Insulating dielectric

SiO_2 → SiOF → CDO (low-k)



Future Options

Ultra Low-k Dielectric

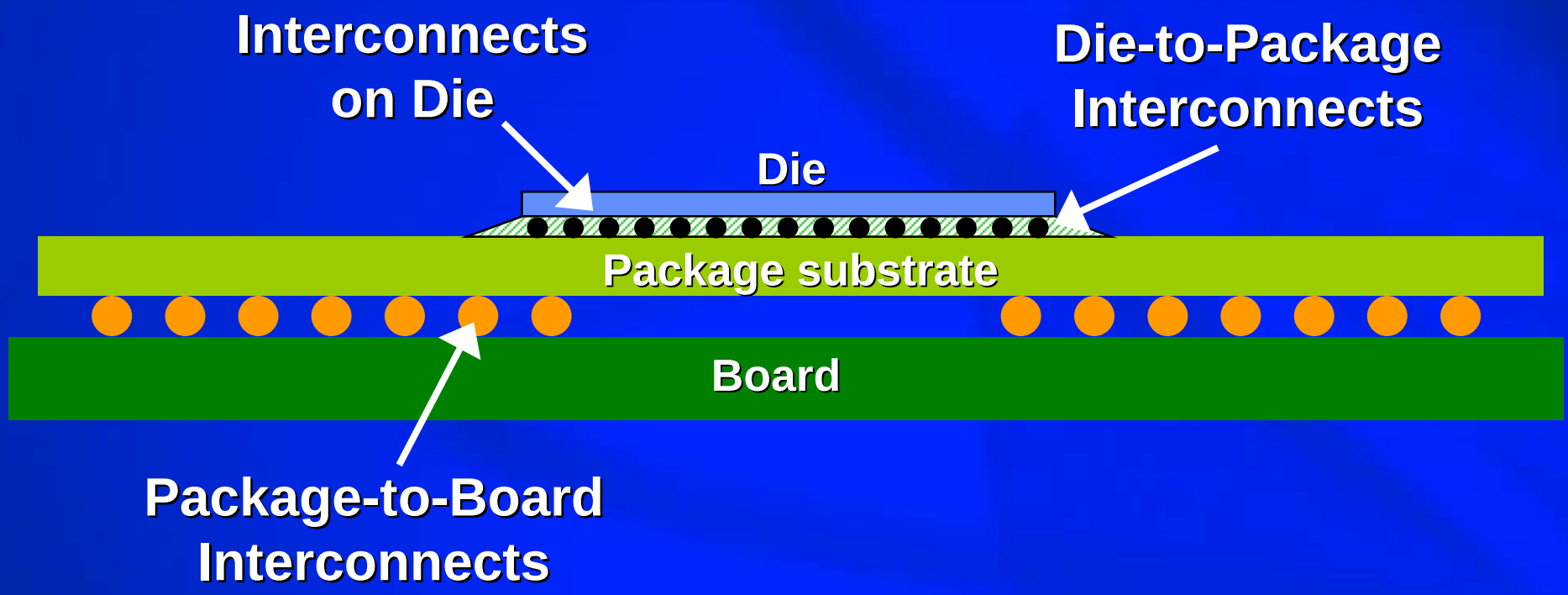
Interconnects

Source: Intel

intel

Die/Package Integration More Critical

Points of Vulnerability:

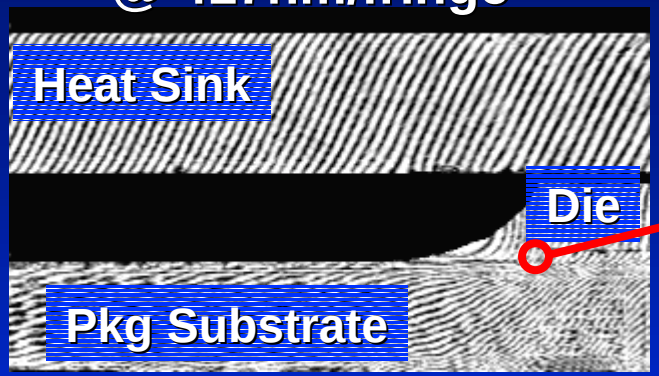


Materials and structures must withstand thermal-mechanical stresses

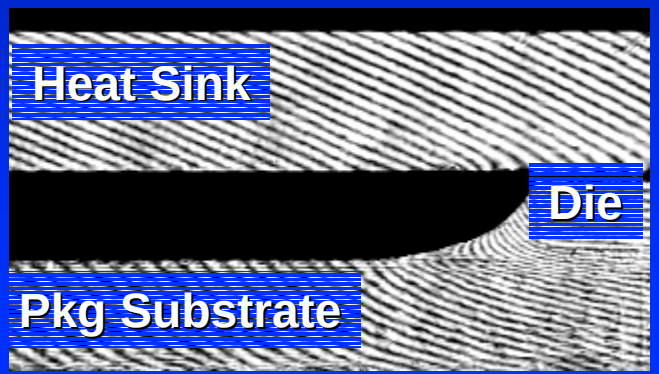
Analytical Tools For Nanotechnology

Package/Interconnect Deformation Measurements

Conventional Moiré @ 417nm/fringe

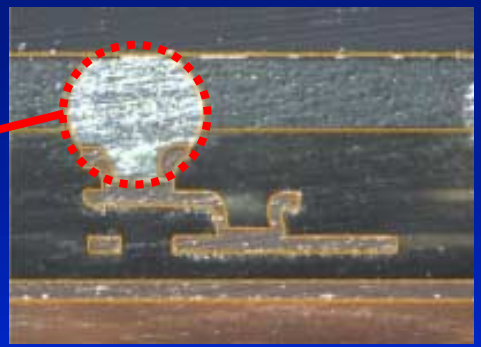


V-field (Vertical Displacements)

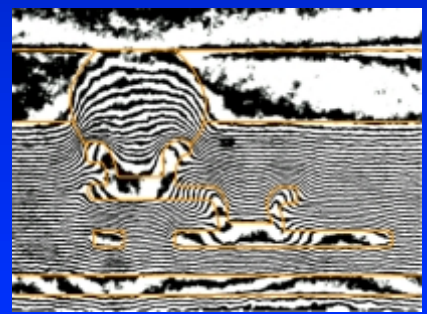


U-field (Horizontal Displacements)

Micro-Moiré @ 52 nm/fringe



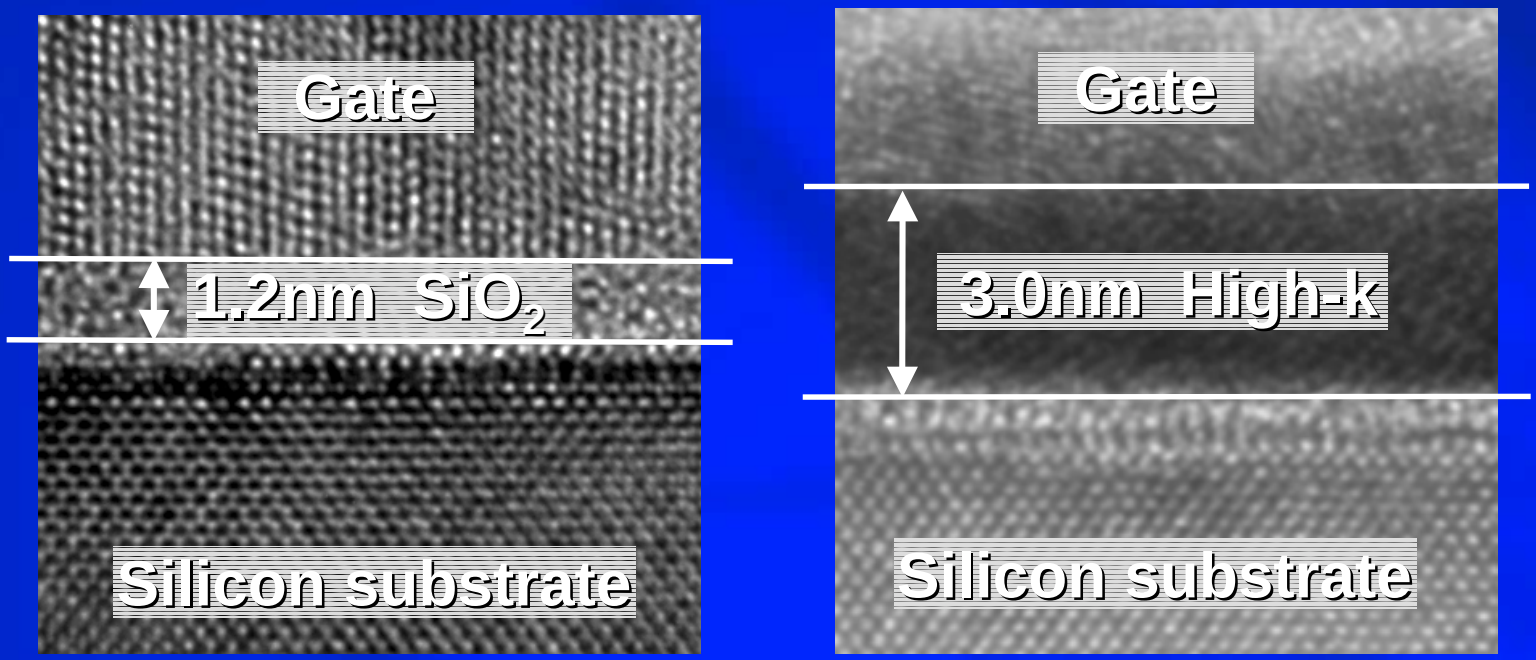
U-field (Horizontal)



V-field (Vertical)

Source: Intel

Nanotechnology for Gate Dielectrics

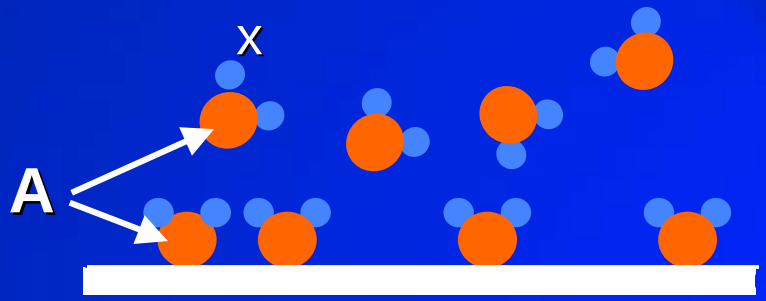


Source: Intel

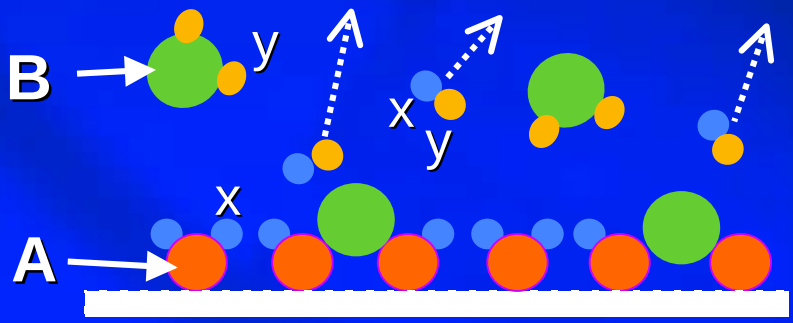
	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Integration is the key challenge

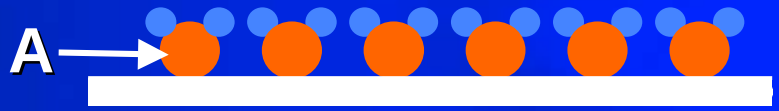
Crafting Films with Atomic Layer Deposition



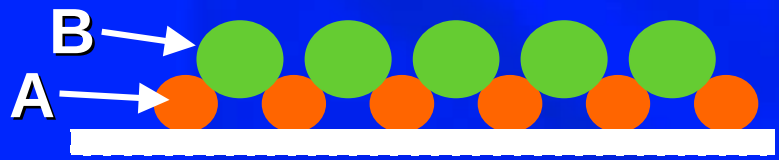
Step 1



Step 3



Step 2



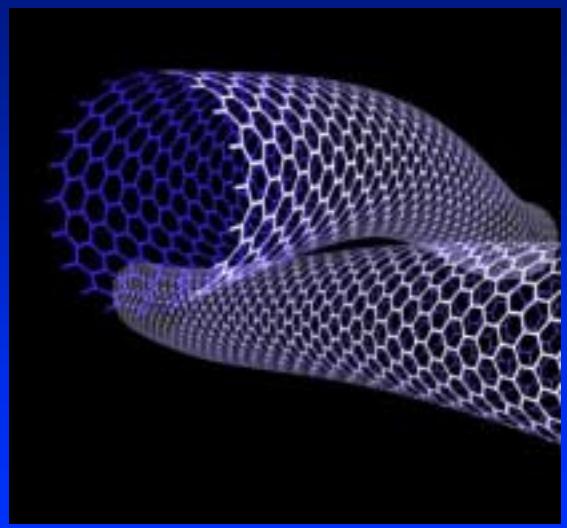
Step 4

ALD: Today's nanotechnology for self-assembly by atomic layer

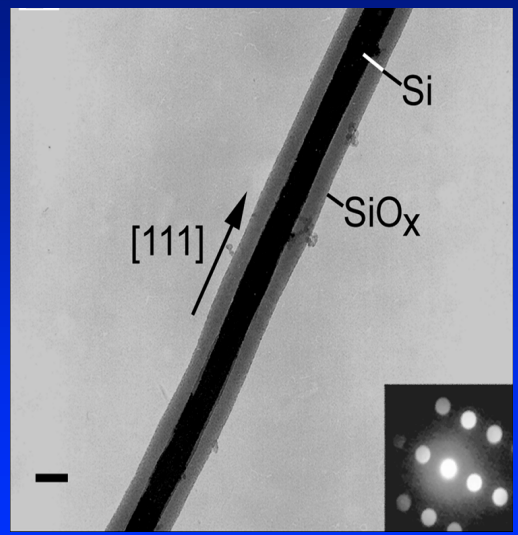
Nanotechnology Futures (> 2010 ?)

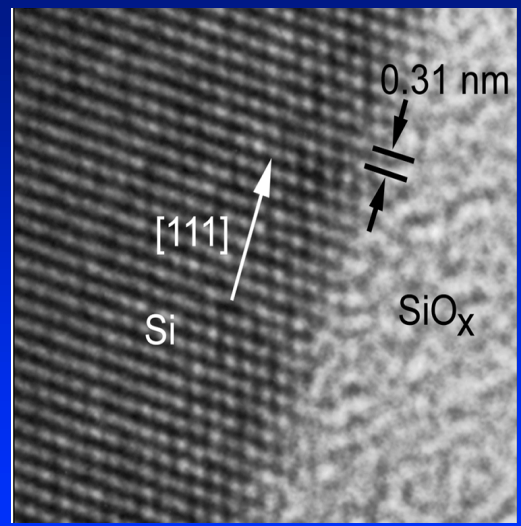
- **Many options including nanotubes/nanowires**
- **Collaborations with universities in progress**

Carbon Nanotube



Silicon Nanowire

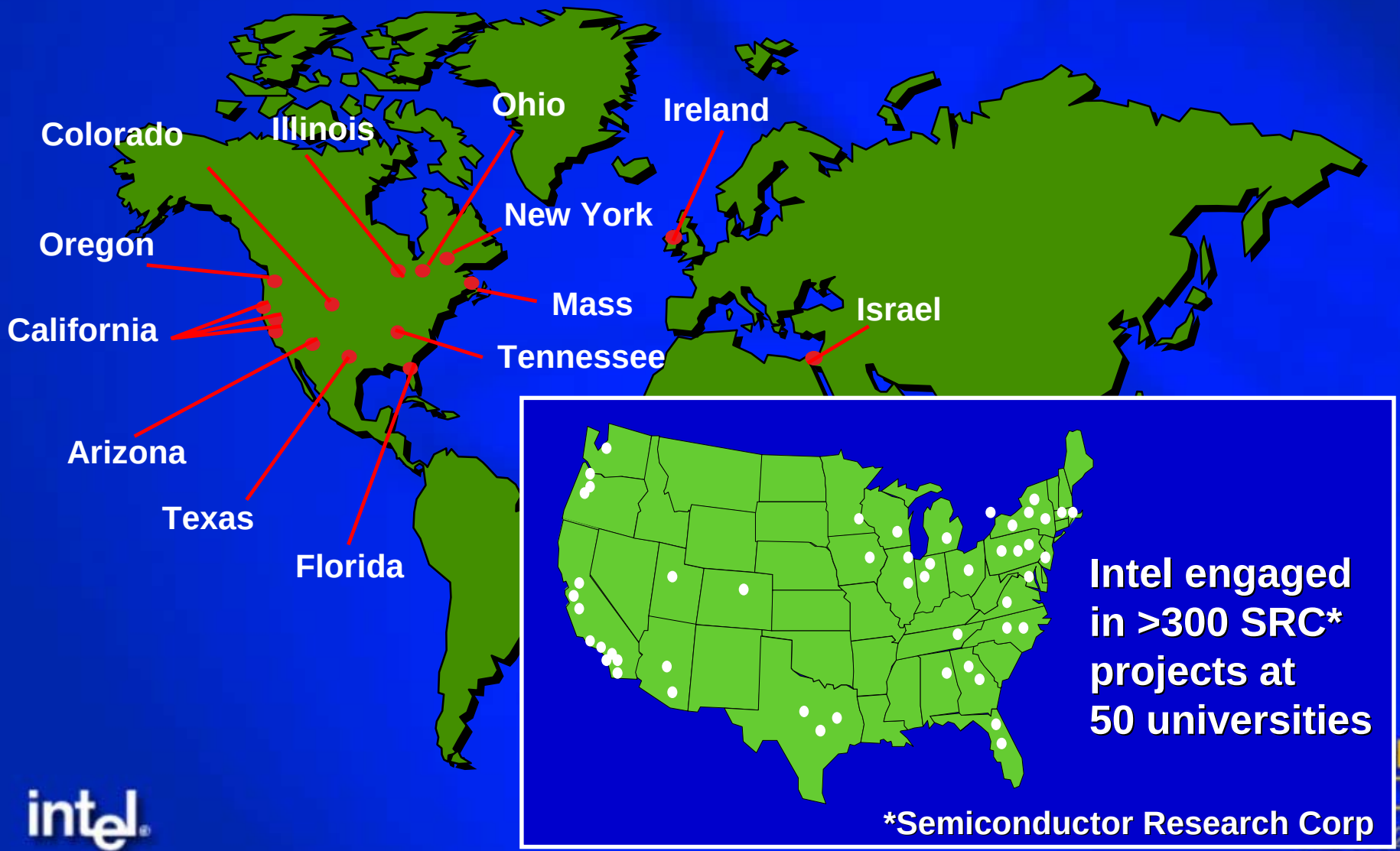




Source: Morales & Lieber, Science **279**, 208 (1998)

Intel Involved in University Research

Intel-supported Nanotechnology Research at Universities



Speeding Nanotechnology to Production

Linking 300mm Research, Development, Production

D1C: 300mm
130nm Production
90nm Development

D1D: 300mm
65nm Development

RP1: 300mm
Research

Source: Intel

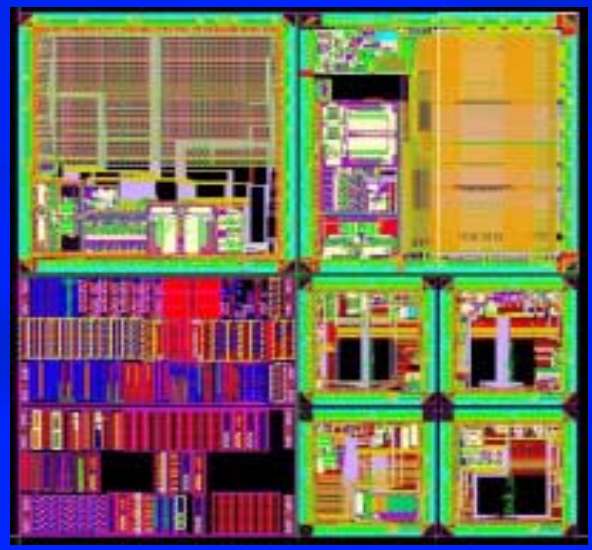
Nanotechnology for Computing and Communications

Process Development Test Vehicles

52Mb SRAM

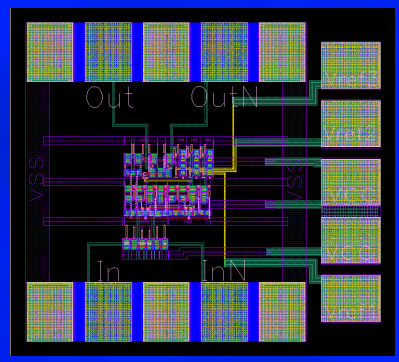
For Processors

WCDMA Analog/RF circuits



For Wireless (Cellular)

40 Gb/s SiGe test circuit



For Optical Communications

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Intelligent Silicon

Nano is Here

New **Devices**, **Materials**, and **Processes**

Sensors

Optical

EXPANDING

EXTENDING MOORE'S LAW

Discrete SSI LSI VLS

Nano

Wireless

Mechanical

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Intelligent Silicon

Nano is Here

New **Devices**,
Materials, and **Processes**

Expanding the Silicon **Canvas**

EXPANDING

Sensors

Optical

Wireless

EXTENDING MOORE'S LAW

Discrete SSI LSI VLS

Nano

Silicon Innovation Enabling Convergence

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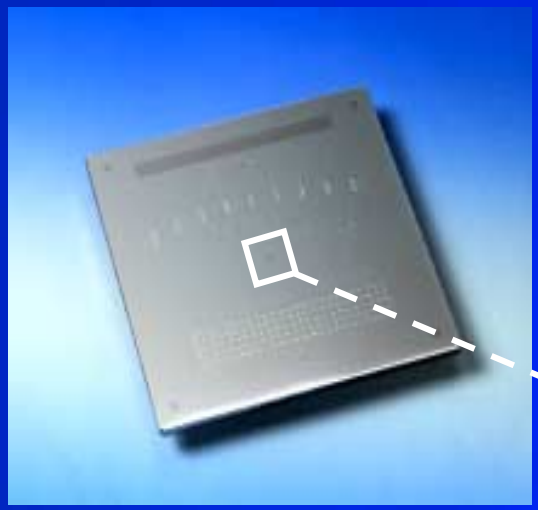
A Piece of Nanotechnology



EUV mask

80-layer EUV reflective coating on thin substrate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